Printed and Electrochemically Gated, High-Mobility, Inorganic Oxide Nanoparticle FETs and Their Suitability for High-Frequency Applications

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Solution-processed or printed n-channel field-effect transistors (FETs) with high performance are not reported very often in the literature due to the scarcity of high-mobility n-type organic semiconductors. On the other hand, low-temperature processed n-channel metal oxide semiconductor (NMOS) transistors from electron conducting inorganic-oxide nanoparticles show reduced-performance and low mobility because of large channel roughness at the channel-dielectric interface. Here, a method to produce ink-jet printed high performance NMOS transistor devices using inorganic-oxide nanoparticles as the transistor channel in combination with a 3D electrochemical gating (EG) via printed composite solid polymer electrolytes is presented. The printed FETs produced show a device mobility value in excess of 5 $cm^2 V^{-1} s^{-1}$, even though the root mean square (RMS) roughness of the nanoparticulate channel exceeds 15 nm. Extensive studies on the frequency dependent polarizability of composite polymer electrolyte capacitors show that the maximum attainable speed in such printed, long channel transistors is not limited by the ionic conductivity of the electrolytes. Therefore, the approach of combining printable, high-quality oxide nanoparticles and the composite solid polymer electrolytes, offers the possibility to fully utilize the large mobility of oxide semiconductors to build all-printed and high-speed devices. The high polarizability of printable polymer electrolytes brings down the drive voltages to ≤1 V, making such FETs well-suited for low-power, battery compatible circuitry.

1. Introduction

Solution-processed and potentially printable FETs have been of high interest in recent years because of a set of new application possibilities that have grown over the last decade which include radio-frequency identification tags (RFIDs),[1] smart packaging, electronic toys, smart textiles,[2] electrophoretic displays,[3] artificial skins[4] and many more. Solution-processability of electronic materials is a prerequisite for the above mentioned functionalities and therefore solution-compatible organic semiconductors have been the primary choice as the active material for solution-processed devices.[5] Organic semiconductors are, however, predominantly p-type, the figure of merit of a FET device, the field-effect mobility (μ_{FET}) is found to vary between 0.1 to 0.6 $cm^2 V^{-1} s^{-1}$ for the best reported solution-processed or printed organic field-effect transistors (OFET).[6,7] This value of mobility is close to amorphous silicon (0.5–1 $cm^2 V^{-1} s^{-1}$) and is adequate for some of the typical applications, however, a successful logic element would also need n-type metal-oxide-semiconductor field-effect transistor (MOSFET) devices (NMOS) in order to build a complementary logic to enhance the signal gain and reduce power loss.[8] Unfortunately, there are not many reports of high performance NMOS devices in the literature from electron conducting organic semiconductors which can match the performance of the PMOS.[9,10] Solution-processed n-type OFETs usually show limited air-stability and a comparatively smaller value of device mobility, $\mu_{FET} \sim 10^{-1}$–10^{-2} $cm^2 V^{-1} s^{-1}$.[10,11]

In contrast, inorganic oxide semiconductors are usually not only electron conducting but are also often endowed with transport properties much superior to any organic semiconductor reported to date. For high quality crystalline oxide semiconductors intrinsic mobility larger than 100 $cm^2 V^{-1} s^{-1}$ is not at all uncommon.[12–15] However, compared to OFETs quite insignificant number of attempts are known in the area of printed logics from oxide materials. The reservations are mostly due to the inorganic materials' inability to simultaneously suit low processing temperature and solution-processing. Solution-processed and printable FETs from inorganic precursors often show high performance, but mostly high processing temperatures are involved which are larger than the glass transition temperature of commonly used inexpensive polymeric substrates.[16–18]

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However, most of the anticipated applications require inexpensive substrates along with low-cost materials and processing and hence the use of paper and plastic as substrates is mandatory. Although, some fascinating recent publications show further successes in reduction of process temperature while maintaining the high performance of the solution-processed oxide TFTs;[19–21] unfortunately, the working temperatures are still not low enough to be compatible to the low-cost polymers (such as polyethylenterephthalat (PET) or polyethylene naphthalate (PEN)) or cellulose substrates. In contrast, the other method to realize inorganic TFTs via solution-processing and printing is by the use of nanoparticle dispersions. With the advancement of nanotechnology, there are presently numerous ways to produce high-quality nanodispersions with small and monodispersed agglomerate sizes. However, these nanodispersions, if not heavily stabilized by functionalization of the particle surfaces, always contain a significant fraction of agglomerates that are at least several times larger than the primary particle size and thereby produce large interface roughness between the transistor channel and the gate insulator; the interface roughness in turn creates charge traps which hinder charge transfer from drain to source. Consequently, the ineffective gating (inhomogeneous field at the channel/dielectric interface) results in device mobility values of only 10^{-2}–10^{-3} cm^2 V^{-1} s^{-1}, four to five times lower than the intrinsic mobility value, characteristic for these materials.[22,23] When agglomerates are avoided with heavy functionalization and a smooth interconnected nanoparticulate monolayer is obtained with spin coating of small-sized nanoparticles (e.g., 5 nm, ZnO) such interface roughness effects can be largely eliminated,[24] however, the semi-insulating nature of the stabilizer at the interface still hinders the electronic transport. With the heavy functionalization, nevertheless, a reasonable value of transistor mobility of nanoparticle-channel ZnO transistors of around 0.6 cm^2 V^{-1} s^{-1} has recently been reported.[24] However, there is not much hope to improve this number any further; moreover, it may be difficult to reproduce such a high-quality nanoparticulate monolayer by any existing printing technique.

In contrast, here we report that ink-jet printed NMOS devices fabricated from heavily-doped inorganic semiconductor nanoparticles with a device mobility $\mu_{FET} > 5$ cm^2 V^{-1} s^{-1} is possible with commercially available nanoparticles, stabilizers and commercial ink-jet printers when an electrochemical top-gating is utilized. The average primary particle size (d_{avg}) of the oxide nanoparticles (Sn-doped indium oxide, ITO) used in this study is 13 nm which resulted in a channel roughness (R_{rms}) in excess of 15 nm. Nevertheless, the composite solid polymer electrolytes can easily follow the surface roughness when printed as a liquid which then solidifies by evaporation of excess solvent. Along with a high value of mobility there are additional advantages of using a polymer electrolyte for gating: a) easy and inexpensive processing, compatible with solution casting and other dispensing techniques such as ink-jet printing; b) besides the conformity of the electrolyte with an extremely rough nanoparticulate channel, it also offers a full penetration of the porous channel resulting in a surround-gate which is surely more effective than the flat gate dielectric geometry; and c) large polarizability of composite polymer electrolytes reduces the operating voltage to ≤1 V, making such transistors battery compatible, and opens possibilities for many novel applications.

Despite all these positive features of electrochemical gating, this approach is only explored by a limited number of researchers around the world; the accelerated activity in this area is mainly impeded by the wide-spread belief that the traditional dielectric of a transistor when replaced by an electrolyte would always make such a device extremely slow and not useful for any practical purpose. Therefore, a main objective of this study is also to show that (at least) for the long-channel, printed transistors electrochemical-gating does not limit the operation speed. With the present-day available printing techniques, unless a rapid development in printer performance shoves the printing resolution and accuracy to a far lower level, the upper limit of usable frequency for the nanoparticle-channel electrochemically-gated FETs would always be governed by the smallest printed channel lengths and the shortest distance of overlap with high-conducting passive structures and not by the ionic conductivity inside the electrolytic-insulators.

2. Results and Discussion

Passive structures of the in-plane transistor device are made of 300 nm sputtered ITO (with sheet resistance of 0.5 Ω $\square^{-1}$) on high quality float glass substrate. The ITO layer is then structured with e-beam lithography to create the source, the drain and the gate electrodes, respectively. The nanoparticle ink is prepared from ITO nanoparticles (Evonik GmbH) with an average primary particle size of 13 nm and a commercially available stabilizer TEGO 752W (Evonik GmbH). The prepared ITO nanoink is printed using a commercial ink jet printer (Dimatix DMP 2831) to bridge the gap between the drain and source electrodes, followed by printing of the water based polymer electrolyte (PVA+KF+H_2O) which covers the nanoparticulate channel completely and the in-plane gate electrode partially. We have already reported in our earlier work,[25] using undoped indium oxide nanoparticles that the development of nanodispersions or nanoinks is possible without an addition of any typical, polymeric stabilizer which enables complete room-temperature processing. However, in this manuscript our intension is to demonstrate something else than complete room temperature processing; namely, a) EG can accommodate very large channel roughness in excess of 15 nanometers and b) the speed of the electrochemically-gated FETs should not usually be limited by the ionic conductivity of the electrolytes even when device mobility of the semiconductor exceeds 5 cm^2 V^{-1} s^{-1}; it is the printing resolution that would determine the frequency limits for these type of devices. Therefore, a commonly-used commercial stabilizer is made use of; however, due to the semi-insulating nature of the stabilizer TEGO 752W, it was essential to remove the stabilizer prior to the electrolyte printing by an annealing performed at 400 °C for 30 min.

2.1. Microstructure and Morphology of Printed Layer

The microstructure and surface morphology of the printed area is summarized in **Figure 1**. Figure 1a,b show scanning and transmission electron microscopy (SEM, TEM) images of a typical printed area. The SEM is performed on an ink droplet,

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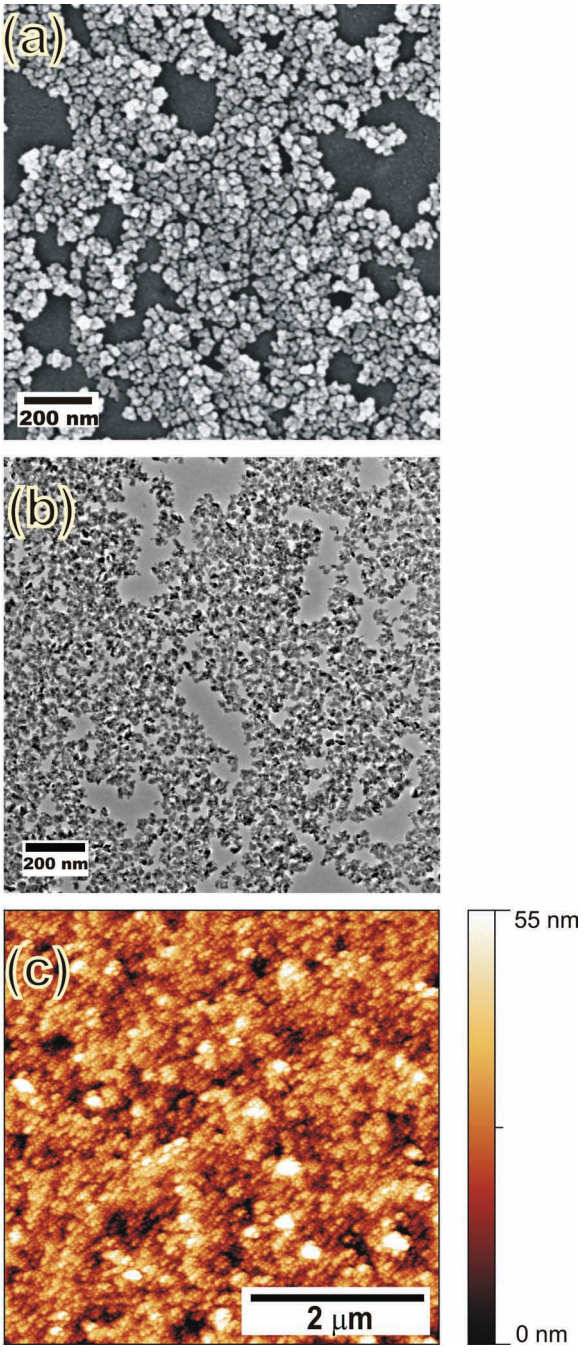

Figure 1. a) SEM image of a typical printed ITO nanoink droplet on plasma-cleaned glass substrate. b) Transmission electron microscopy image of a similar printed ITO droplet on a piranha cleaned TEM grid with 10 nm free-standing Si_3N_4 membrane. c) AFM image of printed ITO drops on plasma-cleaned glass substrate showing individual particles and small, few-particle agglomerates.

which is printed on an identical plasma-cleaned glass substrate, similar to the one used for the device fabrication (Figure 1a). In contrast, the TEM samples are prepared by printing droplets on piranha-cleaned (75% conc. H_2SO_4, 25% H_2O_2) TEM grids with 10 nm free-standing silicon nitride films (Figure 1b). The piranha treatment helps to create a hydrophilic surface and similar surface energy as compared to the plasma-treated glass substrates. The similar surface conditions can be corroborated by comparing very similar printed patterns obtained on both the substrates (Figure 1a,b). In general, it has been found that the printed areas do not show a thick and dense film. The large fraction of the uncovered area that can be seen in the electron microscope images results from the low particle loading and low contact angle of the ink with the hydrophilic substrates. On the other hand, the covered part of the printed droplets are found mostly 1–2 particles in height and with the crest areas showing a maximum 50–60 nm thickness (Figure 1a,b) (this max. thickness of the layers has also been corroborated by extensive profile measurements with Dektak 6M stylus profilometer). Besides low particle loading, the limited layer thickness of the printed films also results from the absence of large agglomerates in the high-quality nanoink, where most of the particle loading is attributed either to single particles or small agglomerates ≤50 nm (Figure S1c, Supporting Information). The atomic force microscopy (AFM) image (Figure 1c) of a similar printed droplet as shown in Figure 1a, shows a little different morphology. The primary particles appear bigger (20–25 nm) compared to what has been observed through TEM (d_{avg} ~13 nm; Figure 1b and Figure S2, Supporting Information), and the overall structure looks denser with a smaller amount of bare areas on the substrate. This can be explained as an effect of the large (~15 nm) radius of the AFM tip, which is easily larger than the primary particle size, after having been used in the tapping mode for a little while. This effect is responsible for the image of the complete structure to look blurry and all features to appear bigger than the actual size. Consequently, not all uncovered areas seen in Figure 1a,b are revealed by the AFM scan. More than 10 AFM frames with 1–5 μm frame size are taken on several droplets. The root mean square roughness (R_{rms}) is found to vary between 13–19 nm. With the AFM tip radius being comparable to the average primary particle size, d_{avg}, the surface roughness of the printed droplets can be underestimated; however, an assessment of R_{rms}, close to d_{avg} may be quite reasonable for layers with homogeneous particle coverage, occasional uncovered areas and a few relatively small agglomerates.

2.2. FET Characterization

The schematic diagram and the electrical characterization of a typical electrochemically-gated ITO nanoparticle channel FET is shown in **Figure 2**; all the electrical measurements have been performed at room temperature (RT) under ambient conditions. The device geometry, as shown in Figure 2a and already described in the earlier section consists of a thin (one-to-two particles in height and with large uncovered areas as well) layer of ITO nanoparticles which is subsequently covered by the printed droplet of the composite polymer electrolyte. Although, the ITO nanoparticulate film is not very homogeneous and shows incomplete coverage of the glass substrate; owing to the large conductivity of individual particles and sufficient inter-particle contacts, the ITO nanoparticulate channel (width:length= 80:10 μm) exhibits a substantial conductivity,

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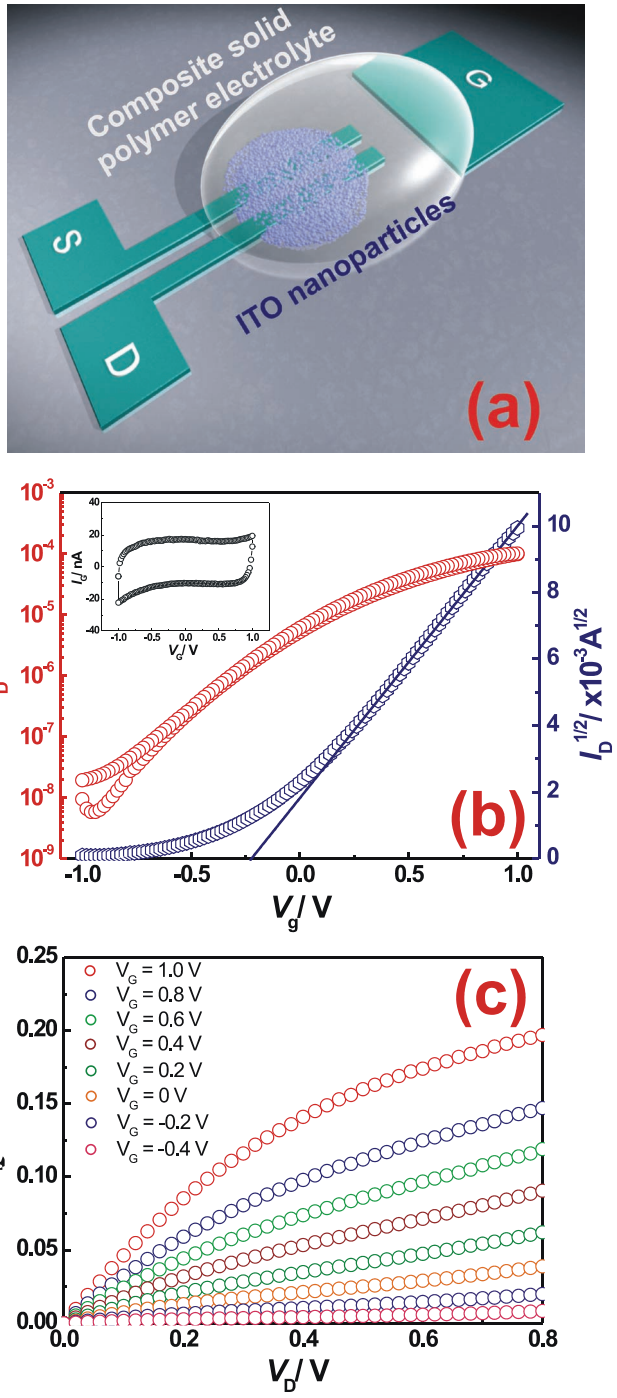

Figure 2. a) A schematic representation of the ITO nanoparticle channel FET device; shows the position of the respective electrodes, the printed layer of ITO nanoparticles and the printed composite solid polymer electrolyte droplet. b) Transfer characteristics of composite solid polymer electrolyte gated, ITO nanoparticle channel FET. Applied drain voltage, V_D = 0.2 V; threshold voltage is calculated to be –0.22 V. Gate voltage is swept with a speed of 1 V s^{-1}. The inset shows the recorded gate leakage during the gate voltage sweep. c) Output (I_D – V_D) characteristics of the device.

i.e., a channel resistance of around 35 kΩ at zero gate potential applied (Figure 2b). Therefore, the transistor channel is being normally-on and ITO being an electron conductor a negative gate voltage is required to squeeze the channel to the Off-state. In fact, with a negative gate voltage (V_g) of –1 V, it is found possible to close the channel to result in a drain current (I_D) of only a few nA. Therefore, the device is similar to a depletion-mode, n-type MOSFET. This is further supported by the negative value (–0.22 V) of the calculated threshold voltage (V_T). When V_g is varied between ±1 V, a change in channel conductance of more than four orders of magnitude is recorded (On/Off ratio >2 × 10^4). ITO, the best-known transparent conductor is renowned for its large carrier density between 10^{20}–10^{21} cm^{-3}; therefore, such a large variation in channel conductance is highly surprising and may only be possible with electrochemical gating which offers large specific capacitance of several μC cm^{-2}. The calculated transconductance ($g_m W^{-1}$) and the current density ($I_D W^{-1}$) at on-state are also found to be notably large (at V_g = +1.0 V and V_D = 0.8 V); 3.12 μS μm^{-1} and 4 μA μm^{-1}, respectively. However, it is not possible to pinch-off the channel completely as can be seen from the drain voltage-drain current characteristics which show the absence of a clear saturation regime (Figure 2c). The graph at the inset of Figure 2b shows the gate current recorded during the gate voltage sweep. Nearly constant value of the gate current suggests that it has mostly resulted from the capacitive charging current of the channel and the connecting electrodes (drain, source) while redox reactions (gate leakage) are essentially suppressed. The choice of a small potential window (V_g = ± 1 V) ensures that only electrostatic field-effect occurs and not any chemical doping at the interfaces. The restriction of the chemical reactions at the interface is important to ensure faster switching of such FETs. On the other hand, the large value of the charging currents (I_g) have resulted mostly from the large parasitic capacitance of highly conducting passive structures with large double layer capacitance (DLC) which are also partially in contact with the electrolyte. This problem can be addressed by a different design of the device, with a better control over the printing processes and surely with an improved printing resolution. In fact, in our device, the overlap area can be close to an order of magnitude larger than the area of the channel due to the resolution-limitation of the printing process itself and mainly due to the spread of the water-based electrolyte on the hydrophilic substrate. Therefore, by comparing the charging currents (Figure 2b, inset) and the Off-current (Figure 2b) of the device, it can be inferred that the Off-current is limited by the capacitive currents due to the large overlap and a lower value should result from a reduction in the parasitic currents.

The field-effect mobility (μ_{FET}) of the device is found larger than 5 cm^2 V^{-1} s^{-1} when calculated with a flat-channel approximation, using the following equation:[26]

$$I_{D,sat} = \frac{W}{2L}\mu_{FET} C (V_G - V_T)^2 \quad (1)$$

where, W/L = 8:1; the specific capacitance (C) is considered to be equal to the double layer capacitance (C_{dl}) of ITO in the composite solid polymer electrolyte, which is measured with sputtered ITO thin film parallel plate capacitors. The schematic of the ITO/electrolyte/ITO capacitor cell is shown in **Figure 3**a. To prepare the parallel plate capacitors, the composite solid polymer electrolyte is added between the

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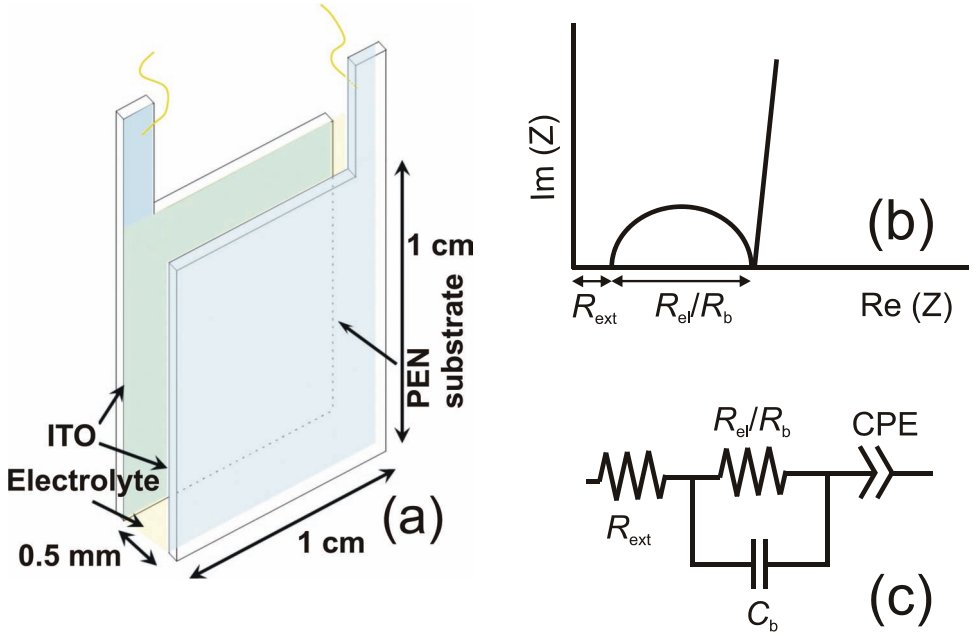

Figure 3. a) Schematic of a parallel plate ITO/electrolyte/ITO capacitor; b) schematic of a Nyquist plot of an ideally polarizable electrode, and c) equivalent circuit model followed in this study for such a blocking, i.e., ideally polarizable electrode system.

ITO electrodes in its liquid state and has been allowed to dry in-situ. The area of the ITO electrodes used is 1 cm^2 and the distance between the capacitor plates are kept approx. 0.5 mm. AC electrical impedance spectroscopy (EIS) is performed with this cell (Figure 3a) for a frequency range of 500 kHz to 1 Hz. A peak-to-peak AC voltage of 10 mV was applied with respect to the open circuit potential (OCP); for both the electrodes made of ITO the OCP was in fact zero volts. Before getting into the details of the recorded impedance spectrum, it is both helpful and necessary to explain the equivalent circuit model used in the present study to analyze the impedance results (Figure 3b,c). As already mentioned in the text that in order to exclude the presence of any redox reactions; non-adsorbing supporting electrolyte (potassium fluoride, KF) has been used in the present work. This fact is further supported by the constant gate current in the I_g–V_g diagram (Figure 2b, inset) which shows predominant capacitive charging and negligible Faradaic currents, even for a large potential window of ± 1 V. Therefore, the impedance model that we have chosen for this study is the simplest one; involving a blocking or in other words an ideally polarizable electrode, i.e., an electrochemical cell in absence of any Faradaic current (Figure 3c).[27] Therefore, the model we have considered here consists of an external resistance (R_{ext}); this considerable value of resistance has actually resulted from our cell design, from the long narrow ITO leads (Figure 3a) and can usually be neglected for highly conducting electrodes; then comes the bulk or electrolyte resistance (R_b/R_{el}) and the bulk capacitance (C_b) in parallel. This bulk capacitance appears from the dipolar relaxation of the electrolyte solvent molecules; however, the value is usually negligible, only in the order of 10^{-10} F cm^{-2}, when compared to the double layer capacitance (C_{dl}) (Table S1, Supporting Information). Lastly, the double layer capacitance is in series with the other components; however, owing to the fact that in reality a perfect or ideal capacitor can never be found (as is also evident from the near vertical linear region in the low frequency part of the Nyquist plot (Figure 3a and **Figure 4**a)), the C_{dl} in the equivalent circuit model is replaced by a so-called constant phase element (CPE). While, a perfect capacitor would result in a vertical line with a phase angle, ϕ of 90°, a linear region with a little lower than 90° phase angle signifies a slightly non-ideal capacitive behavior which can easily be accounted by a CPE when added to the equivalent circuit model. However, it may be important to note here that C_{dl} only slightly deviates from the ideal capacitive behavior as can be seen from the fitting of the experimental data (Figure 4a) with the above mentioned model (Figure 3c) which gives CPE being always more than 90% capacitive. The experimental EIS data (open red circles) along with the fitting (blue lines) are shown in Figure 4(a–c). It can be seen in Figure 4 that for both the Nyquist plot and the Bode plots, a quite satisfactory fit is obtained with this simple model. The electrolyte resistance, as shown in Figure 3b, calculated by subtracting the external resistance, R_{ext}, from the Re(Z) at the minimum phase angle, is found quite reproducible for six different parallel plate capacitor cells, with varying electrode surface area and inter-electrode spacing, which have been measured. In fact, high degree of reproducibility is observed as the conductivity values are found always in the range of 2×10^{-5} S cm^{-1} which are then averaged for all the cells in order to provide $\sigma_{avg.} = 2.3 \times 10^{-5}$ S cm^{-1}. The conductivity of the water-based composite solid polymer electrolyte used in this work is found to be comparatively low; primarily the reason behind such low conductivity may be due to the low boiling point and high vapor pressure (~20 mmHg) of H_2O at RT, which resulted in a low water (solvent) content in the final form of the dried electrolyte films.

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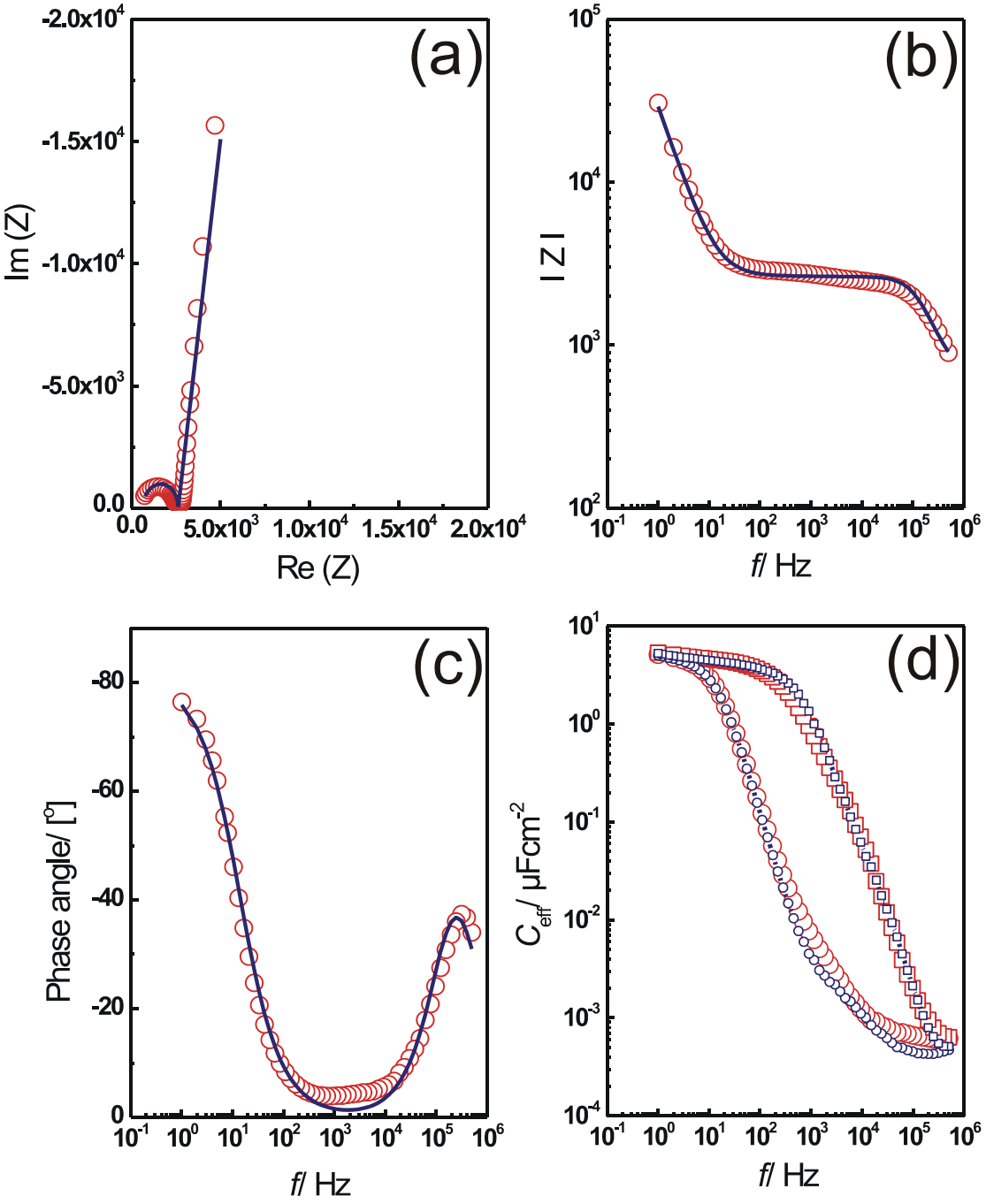

Figure 4. a) Nyquist plot of the ITO/electrolyte/ITO electrochemical, parallel plate capacitor recorded for a frequency range of 500 kHz to 1 Hz; b) the total impedance, and c) phase angle obtained from the experimental data. a–c) The red circles and the blue lines denote the experimental and the fitted data, respectively. d) The calculated effective capacitance for two independent cells (red and blue symbols) are plotted where the C_{eff} is calculated by using Equation (2) (squares) and Equation (3) (circles), respectively.

2.3. Calculation of Effective Capacitance Versus Frequency

As already mentioned in the previous section, the calculation of the device mobility requires a precise and accurate knowledge of capacitance; however, it is also very important to examine the variation of effective capacitance (C_{eff}) of an ITO/solid polymer electrolyte/ITO parallel plate capacitor versus frequency in order to assess the viability of such electrochemically-gated FETs at higher frequencies.

In fact, attempts to calculate C_{eff} with respect to varying frequency have been made in the past. In many previous publications that relate to electrochemical gating plots of C_{eff} vs.

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frequency of electrode/electrolyte/electrode parallel plate capacitors have been presented. However, in all those previous reports either the calculation of C_{eff} vs. frequency was not discussed in greater details[28–32] or it had been calculated using the following equation:[33–37]

$$C_{eff} = -(\mathrm{Im}Z \times \omega)^{-1} \quad (2)$$

where, ω is the angular frequency (= $2\pi f$).

However, we believe that this equation is valid only for very low frequencies where the phase angle, ϕ is close to 90°; the estimation of C_{eff} becomes increasingly erroneous and overestimated with increasing frequency and decrease in the phase angle, where the close to ideal capacitor starts to become increasingly resistive. Stated differently, Equation (2) does not account for voltage drop at the real part of the total impedance i.e., the electrolyte resistance which is increasingly important at higher frequencies. Due to this ohmic electrolyte resistance the "double layer capacitor" accumulates less and less charge with the increasing frequency. In fact, at $\mathrm{Re}(Z) = R_{el}$ (see Figure 3b), the total impedance mostly consists of the electrolyte resistance and thus the effective charge at the gate becomes negligible.

Therefore, we have formulated an equation to calculate the effective capacitance by integrating the charging current from peak-to-peak voltage (thereby accounting for the voltage drop at the electrolyte resistance; see Supporting Information Figure S3). Following this approach, we arrive at Equation (3):

$$C_{eff} = -\frac{\mathrm{Im}Z}{\omega |Z|^2} \quad (3)$$

In Figure 4d, C_{eff} vs. frequency is plotted where C_{eff} is calculated for two different capacitor cells (again to show the performance reproducibility) which are shown by the red and blue symbols, respectively. Figure 4d clearly denotes a large difference between C_{eff} values calculated using Equation (2), (red and blue squares) and Equation (3) (red and blue circles), respectively. It can be easily seen that at very low frequencies both equations give identical values, because at that low frequency the charge double layer is fully formed which is evident from the large, close to 90°, phase angle (Figure 4c), however, for larger frequencies with decreasing ϕ, Re(Z) accounts for an increasingly larger fraction of the total impedance compared to the imaginary part with which Equation (2) becomes increasing erroneous and overestimated. It is important to note that the overestimation that one can make by using Equation (2) cannot be ignored; Figure 4d clearly shows that for frequencies around 10^3 Hz, for the parallel plate capacitor built and measured in this study, the overestimation in calculated C_{eff} can be as large as three orders of magnitude. The impedance results and the correctness of the frequency dependent capacitance calculation using Equation (3) have also been corroborated by the results from cyclovoltammogram (CV) measurements (**Figure 5**). In fact, it is believed that this comparison is quite obvious and straightforward, because analogous to the C_{eff} calculations for the EIS data, effective capacitance from the CV measurements is also obtained by integration of the charging currents in order to compute the accumulated charge at certain scan speed. During the CV measurements, the parallel plate ITO

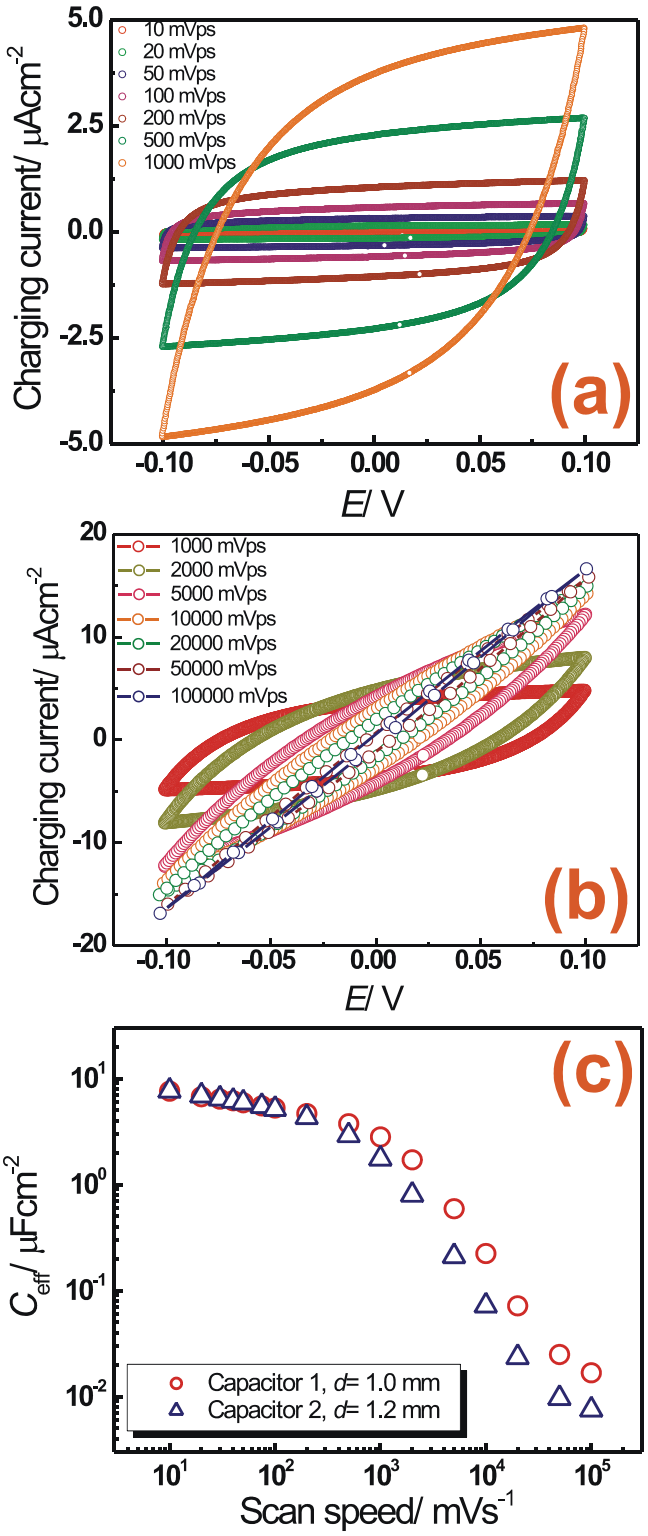

Figure 5. Cyclovoltammograms performed on parallel-plate capacitors made of ITO thin films and water based solid polymer electrolyte (PVA+KF+H_2O). a,b) Scan rates between 10 mV s^{-1} and 1 V s^{-1} and scan rates between 1 and 100 V s^{-1}, respectively. c) Calculated effective capacitance versus scan speed for a couple of such electrochemical capacitors with a slightly different distance between the ITO electrodes.

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capacitors are cycled between ±100 mV with respect to OCP (which is again zero volts, both the electrodes being identical) and the charging current is recorded and integrated over time to obtain C_{eff}. Figure 4a,b show the CV scans for different scan rates where the deviation from the square shape I–V plots and the increasing time to reverse the sign of the charging current (when the direction of the potential sweep is reversed) with an increasing scan speed signifies incomplete charging of the electrodes. Figure 4c illustrates C_{eff} with respect to the scan speed. Table S2 (Supporting Information) shows a comparison between the C_{eff} values obtained from the EIS and the CV data; where (the CV potential window being 200 mV) the C_{eff} values computed from the 200 mV s^{-1}, 500 mV s^{-1}, and 1 V s^{-1} scan rate CV data are compared with 1 Hz, 2.5 Hz, 5 Hz EIS results, respectively. Such comparisons between the EIS and the CV results are not customary, especially, because of the large CV potential window, which is not acceptable as an EIS AC amplitude owing to the possible deviation from the linear response; therefore, it is not the intention here to put an extra stress to the fact that an excellent match in the calculated C_{eff} values has been obtained from both the experimental techniques (Table S2, Supporting Information). However, it is not unreasonable to compare the order of the C_{eff} values obtained from these techniques, which is undeniably sufficient to validate the C_{eff} calculations using Equation (3) from the EIS data.

From the fitting of the Nyquist plot shown in Figure 4a, we obtain the C_{dl} value of 6.7 μF cm^{-2}. However, in order to ascertain the most conservative estimation in the mobility calculation, we have taken C_{dl} = 7.6 μF cm^{-2}, which is obtained from the CV measurement with the slowest (10 mV s^{-1}) scan speed; although, knowing that for such slow scan rates a little Faradaic current may be present which can increase the value of calculated C_{dl}. Coming back to Equation (1), the field effect mobility, μ_{FET}, when calculated with C_{dl} = 7.6 μF cm^{-2} results in a value >5 cm^2 V^{-1} s^{-1}. It should also be noted here that the ITO nanoparticles cover the substrate, only partially (Figure 1), resulting in a limited number of conducting paths, and hence yielding quite an overestimation of the channel widths. This in turn may have reduced the calculated device mobility value considerably.[21] An optimization of the process parameters, such as, a modification of the ink composition and an improvement in the printing quality to obtain denser nanoparticle coverage on suitable substrates are therefore the obvious next steps to increase the On-current and the μ_{FET} further.

2.4. Limiting Speed of EG FETs

Nevertheless, the value of μ_{FET} obtained in this study is nearly an order of magnitude larger than in amorphous silicon and should fulfill all the major application requirements mentioned earlier in this report. However, unfortunately a high value of mobility, alone is not sufficient to ensure high frequency performance. On one hand, a major advantage of EG is the low drive voltage requirement which makes these devices battery compatible and suitable for various portable electronic applications; on the other hand, EG also limits the maximum drain voltage (V_D) to small numbers, in order to restrict the Faradaic currents to negligible values. When the contact resistances (which should any way be negligible for the present device-type) are not taken into account, the cut-off frequency, f_T, (the frequency that results in an unity current gain, a transistor cannot be used at a frequency higher than f_T) of a MOSFET is given by[38]

$$f_T = \frac{\mu_{FET} V}{2\pi L (L + 2\Delta L)} \tag{4}$$

where, V is the drive voltage and ΔL is the length of overlap of the dielectric with passive structures. However, for an all-printed transistor, the channel length and the length of the insulator (printed electrolyte) both are defined and limited by the printing resolution, hence, the overlap area can be considerably smaller than the channel length ($\Delta L < L$), making Equation (4) a little simpler. In this case Equation (4) would reduce to

$$f_T = \frac{\mu_{FET} V}{2\pi L^2} \tag{5}$$

From Equation (5) one can notice that regardless of a very large mobility, the maximum attainable speed of a printed device is always limited by the large channel lengths offered by the printing processes with limited resolution. The importance of the printing accuracy/resolution can be seen for the present device, when an applied drain voltage (V_D) of 1 V ($V = V_D$; as $V_D < V_G - V_T$) results in f_T equal to 32 kHz and 800 kHz for the channel lengths of 50 μm and 10 μm, respectively. Consequently, for printed FETs, not only the high device mobility is crucial but the printing resolution may be far more important to limit the overlap area, hence the overlap capacitance, and moreover to reduce the channel lengths.

Finally, we would like to compare the speed of such printed FETs in terms of semiconductor quality and device geometry (Equation 5) with the speed of the electrochemical capacitors they exploit, in order to examine if actually the speed of these EG FETs is limited by the ionic conductivity of the electrolyte. Often expressed reservations against the electrochemically-gated devices arise from the general conviction that the speed of such FETs would be restricted by the slowly moving ions in the electrolytes and hence a very large mobility value, as in the present case, is of no real advantage. Indeed, such judgments are partially true, the ionic conductivity may not be large in some solid polymer electrolytes; one such example can be the water based composite polymer electrolyte used in this work. Nevertheless, it can be shown that the negligible electrolyte thickness in a printed device (can be as low as 100–500 nm) compared to the large channel lengths (10–50 μm) more than compensates for the low conductivity of the ions in the electrolyte. An equivalent circuit of a two-electrode electrochemical cell with ideally polarizable electrodes is shown in Figure 3c. As a good approximation, the bulk capacitance (C_b) can be ignored due to its negligible numeric value (Supporting Information Table S1, S3) leaving a simple RC circuit as shown in Figure S4. The cut-off frequency (f_C) for such a RC circuit is therefore given by

$$f_C = \frac{1}{2\pi RC} \tag{6}$$

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If we calculate the effective capacitance, C_{eff} at the cut-off frequency (see supporting materials) for such a simplified system, it can be found that at $f_C = 1/2\pi RC$,

$$C_{eff} = \frac{C_{dl}}{2} \quad (7)$$

It would definitely be a safe and conservative estimate, if we define this cut-off frequency, f_C, as the maximum frequency at which such electrochemically-gated transistors will be able to operate; because, half of the double layer capacitance would surely be enough, by far, to cause more than unity current gain. Calculated from the electrolyte resistance and C_{dl}, the cut-off frequency (f_C) for the water-based composite polymer electrolyte approaches to 100 kHz and 20 kHz, for 100 nm and 500 nm membrane thickness, respectively (typical value for printed layers) even when the conductivity (σ) is only of 2.3×10^{-5} Scm^{-1}.

It has already been mentioned in the previous section that the low conductivity of the water-based polymer electrolyte is due to the evaporation of most of the solvent (H_2O) present in it. Consequently, a significant improvement can be anticipated by replacing water with high boiling point and low vapor pressure (at RT) solvents such as propylene carbonate (PC) and dimethyl sulfoxide (DMSO). Indeed, a tremendous improvement in conductivity of the composite polymer electrolytes is possible by using these non-volatile solvents. As an example, the performance of an easily printable non-aqueous solvent based (PC and DMSO) composite polymer electrolyte is shown in **Figure 6**. Especially, PC having a vapor pressure of less than 0.04 mbar is better trapped within the polymeric network giving a much larger conductivity of the electrolyte in its dried form. High conducting composite polymer electrolytes from similar non-aqueous, non-volatile solvents have previously been reported in the literature.[39–41] PC and DMSO based composite electrolytes that we have synthesized show a conductivity in excess of 1.1×10^{-2} S cm^{-1}, which when translated into cut-off frequency (even for a 500 nm membrane) would raise the value to ≥10 MHz, which in any case is far more than what can be achieved by printed transistors with present-day printing techniques and accuracy. It may be noted here that to facilitate an accurate measurement of the electrolyte resistance in such a high conducting electrolyte system, it was necessary to have a small electrode area (0.05 cm^2) and a large distance between the respective ITO electrodes (1.5 cm).

3. Summary

In conclusion, we have demonstrated that printed FETs prepared by combining inorganic oxide nanoparticles as the transistor channel and the composite solid polymer electrolytes serving as the gate insulators, is an interesting approach with future prospects as it can result in transistors with considerably large value of carrier mobility. The surround-gating offered by this concept is far more efficient than traditional dielectric gating when the active layer of the transistor is comprised of a nanoparticle assembly. The electrolyte printed in its liquid state can easily follow the rough surface of a nanoparticulate channel to provide a good channel-insulator interface; the present device

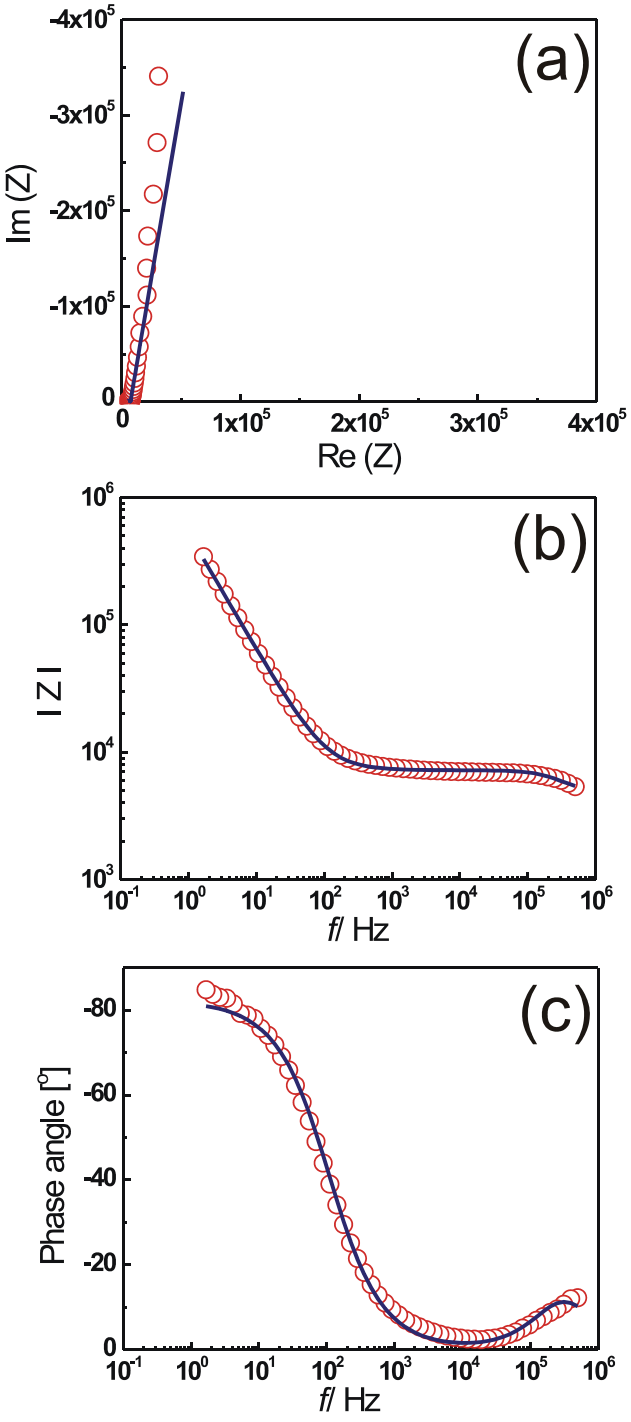

Figure 6. EIS data of the non-aqueous solvent based composite solid polymer electrolyte. a) Nyquist plot of the electrochemical capacitor for a frequency range of 500 kHz to 1 Hz; b) the total impedance, and c) phase angle obtained from the experimental data. a–c) The red circles and the blue lines denote the experimental and the fitted data, respectively. The electrode area and the distance between the ITO electrodes are kept 0.05 cm^2, and 1.5 cm, respectively.

can be taken as a proof of this phenomenon where the printed ITO droplets/layers show a RMS surface roughness larger than 15 nm. Next, an equivalent circuit model and corresponding

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formulation of the effective capacitance for an electrochemical cell involving only ideally polarizable electrodes has been presented which provides a far more realistic estimate of C_{eff} at all frequencies compared to the equation extensively reported in the literature. Finally, the cut-off frequency has been calculated from the semiconductor performance and the device geometry (such as channel lengths) and is compared to the cut-off frequency given by the electrochemical capacitors in consideration, in order to ascertain that even for the water-based solid electrolyte with comparatively poorer ionic conductivity, the maximum attainable transistor speed is not really limited by the charging time of the electrochemical capacitor. Furthermore, when a better conducting electrolyte, such as the high conducting solid polymer electrolyte with PC as a solvent is considered, the capacitor charging time can be lowered down to less than 0.1 µs, i.e., the cut-off frequency of the capacitor raises beyond 10 MHz. This clearly ensures that for the long channel printed FET devices EG does not hamper the transistor performance. Hence, the electrolyte relaxation time is by far shorter than the cut-off frequency that a printed device can reach due to geometrical factors. This in turn signifies that for a long time from now an improvement in printing resolution will remain the key to increase the speed of EG FET devices.

4. Experimental Section

Nanoink Preparation: To prepare the water-based nanoparticulate inks, 10 wt% (1 g) of ITO nanopowders (Evonik GmbH) were added to deionized water (10 ml) which was then loaded with 5 wt% of commercial stabilizer TEGO 752W (Evonik gmbH). The mixture was spun in a home-made dispersion unit based on commercial dissolver/mixer DISPERMAT for 90 minutes at 9000 rpm with 400–600 µm zirconia pearls as the milling media. Next, the dispersion was filtered to separate the pearls and was loaded in 1 ml centrifuge capsules to centrifuge (Eppendorf, Centrifuge 5415D) at 5000 rpm for 5 min. Approximately 650 µl of supernatant fluid was separated carefully and then filtered through a 200 nm PVDF membrane filter to obtain ITO nanoink ready for printing. The size distribution of the agglomerates present in the nanoink was measured with dynamic light scattering (DLS) (ALV-NIBS High Performance Particle Sizer) (Figure S1c, Supporting Information).

Electrolyte Preparation: The water-based composite solid polymer electrolyte consists of a water soluble synthetic polymer, poly(vinyl alcohol), (PVA) of low molecular weight (average mol. wt. = 13 000–23 000) 98% hydrolyzed, Sigma-Aldrich), deionized water as the solvent and a non-adsorbing supporting electrolyte, such as potassium fluoride, KF (Alfa Aesar). Equal amount of PVA and KF was added to deionized water separately and homogenized with constant stirring at 75 °C. The clear solution of KF was then added to the viscous PVA solution and stirred for at least 12–24 h at RT to obtain a completely single phase, clear and homogeneous solution (liquid electrolyte) which was then used as the starting material to print the solid polymer electrolyte.

To prepare the non-aqueous solvent based composite solid polymer electrolyte the polymer (poly(vinyl alcohol) (PVA), average mol. wt. = 13 000–23 000) 98% hydrolyzed, Sigma-Aldrich), the plasticizer (propylene carbonate (PC), anhydrous, 99.7%, Sigma-Aldrich), the supporting electrolyte/salt (lithium perchlorate, $LiClO_4$, anhydrous, 98% Alfa Aesar or sodium perchlorate, $NaClO_4$, anhydrous, 98–102.0% Alfa Aesar) and the solvent (dimethyl sulfoxide, DMSO, anhydrous 99.9% Sigma-Aldrich), were used without further purification. Weight percentage of the following ingredients PVA: PC: $Li/NaClO_4$ was kept 30:63:7. Sufficient amount of DMSO was added (5–6 times of the total weight of the other constituents) in order to ensure the right viscosity value for easy printability. Certain amounts of the composite solid polymer electrolyte were prepared in the following manner: first (0.75 g) PVA was added to (15 g) DMSO and the solution was then stirred and heated continuously at 80–100 °C for several hours until the mixture became a homogeneous solution. Certain quantities of salt (either lithium or sodium perchlorate) (0.175 g) was dissolved in PC (1.575 g) and was added to the PVA solution. The complete mixture was then stirred at RT for at least 12–24 h to obtain a completely single phase, clear and homogeneous solution (liquid electrolyte) which was then used for printing using a Dimatix 2831 ink-jet printer. The electrolyte was filtered through a 450 nm filter (PVDF membrane for the water-based composite solid polymer electrolyte and PTFE membrane for the DMSO-based electrolyte, respectively) prior to the loading in the cartridge for printing.

Printing: The printing was performed using a commercial Dimatix DMP 2831 ink-jet printer with piezoelectric nozzles having a nozzle diameter of 21.5 µm. All the printing steps were carried out at RT on plasma-cleaned and lithographically-patterned 0.7 mm thick high quality float glass substrates. The TEM grids with free-standing 10 nm Si_3N_4 membranes (TEMwindows) were significantly hydrophobic at the as-received condition. Therefore, they were cleaned with piranha solution (75% conc. H_2SO_4, 25% H_2O_2) prior to printing, in order to create identical hydrophilic surface. In fact, when printed on such grids with the same printing parameters (printing voltage and waveform), it was possible to obtain similar printed droplet morphology, droplet size (diameter) and heights as compared to the plasma-cleaned glass substrates which indicates that the piranha treatment also resulted similar hydrophilicity.

Characterization: The nanoparticle arrangement/distribution in the printed area were investigated with a Leo 1530 Gemini scanning electron microscope (SEM), and similar printed areas on the TEM grids were examined with transmission electron microscopy (TEM) using a FEI Titan 80–300 microscope. Atomic force microscopy had been performed with a commercial DI-Nanoscope III (MMAFM-1 model) microscope.

Electrochemical Measurements: Cyclovoltammetry and impedance spectroscopy measurements of the parallel plate ITO/electrolyte/ITO capacitors were performed using a Biologic VMP3 multichannel potentiostat equipped with impedance modules.

Electrical Measurements: The electrical measurements were performed at RT and in ambient conditions. For contacting the electrodes a precision probe station (SÜSS MicroTec MLC-150C) was used. The electrical measurements were carried out with a precision semiconductor parameter analyzer (Agilent 4156C).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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